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TF 2422

300 MHz Divider

INSTRUCTION MANUAL

MP MASTER
MA23660

MARCONI INSTRUMENTS LIMITED

368

INSTRUCTION MANUAL

No. 68B 2422

for

300 MHz Divider

TF 2422

MARCONI INSTRUMENTS LIMITED
ST. ALBANS HERTFORDSHIRE ENGLAND

M.I.L. 22C
33/711/AA

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Chapter 1

General information

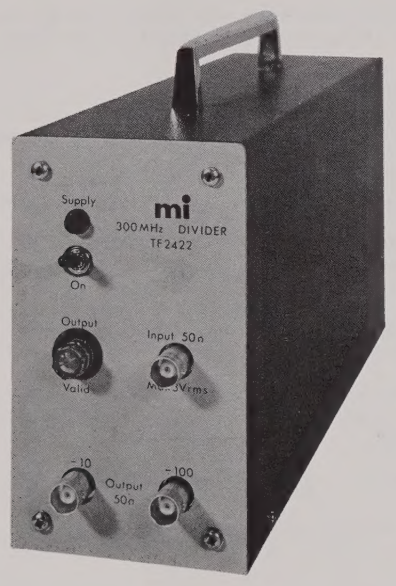


Fig 1.1 300 MHz Divider TF 2422

1.1 INTRODUCTION

The TF 2422 300 MHz Divider enables signals in the range 5 MHz to 300 MHz to be frequency divided by factors of 10 and/or 100; both outputs are available at front panel mounted coaxial sockets.

The instrument may be used as a pre-scaler to provide very high frequency measurement capability for standard frequency measuring instruments/counters having an upper frequency response limited to a few megahertz.

Suitability of the applied input signal and correct frequency division within the instrument is indicated by illumination of a front panel mounted indicator lamp designated 'Output Valid'.

Integrated circuits and other silicon semi-conductor devices are used throughout the instrument which employs plug-in printed circuit boards. The TF 2422 is designed for mains operation and is produced as a bench standing unit fitted with a carrying handle.

1.2 DATA SUMMARY

INPUT

This specification only holds for continuous sinusoidal inputs. A mark/space ratio exceeding 60:40 may result in erroneous operation.

Minimum input for correct operation	25 mV r.m.s. (5 MHz - 300 MHz)
Maximum input for correct operation	3 V r.m.s. (5 MHz - 300 MHz)
Typical frequency range for an input voltage of 60 mV r.m.s. and up to 3 V r.m.s.	100 kHz to 330 MHz
Absolute maximum input a.c. or d.c.	5 V
Input impedance	Nominal 50 ohms
Input connectors	BNC
Division Factors	10 and 100

OUTPUT

Output pulse (a.c. coupled)	Rectangular 1 volt p-p
Mark/Space ratio	2:3
Output impedance	Nominal 50 ohms
Output connectors	BNC
Signal indicator lamp	Illuminated when the instrument is dividing correctly

POWER REQUIREMENTS 100 - 125 V/200 - 250 V
45 - 60 Hz 15 VA

DIMENSIONS and WEIGHT

Width	Height	Depth	Weight
78 mm (3.1 in)	133 mm (5.25 in)	275 mm (10.9 in)	2.5 kg (5.5 lb)

Chapter 2

Operation

2.1 INSTALLATION

The TF 2422 is available only in the bench mounted version. It is despatched set for 200 - 250 V a.c. operation.

2.1.1 Mains Supply 100 - 125 V a.c.

To alter the mains voltage setting for use with 100 - 125 V a.c. supply proceed as follows -

(i) Remove the instrument cover by withdrawing the four pan-head securing screws.

(ii) Locate the mains transformer on the power unit circuit board at the rear of the instrument. (refer to Fig. 5.1).

(iii) Change the split primary tapping of the mains transformer from the 200 - 250 V a.c. operation as shown in Fig. 2.1 to that shown in Fig. 2.2

(iv) Ensure that the rear panel mounted mains fuse is of the correct rating.

250 mA for 200 - 250 V a.c. supply
500 mV for 100 - 125 V a.c. supply

2.1.2 Mains Cable Connection

Connect the mains cable to the supply in accordance with the following colour code:-

Brown	-	Live
Blue	-	Neutral
Green/Yellow	-	Earth

2.2 OPERATION

CAUTION

To avoid damage to the input circuit ensure the input signal does not exceed ±5 V with respect to chassis

Now proceed as follows -

(i) Connect the input signal source via a 50 Ω co-axial cable to the INPUT socket.

(ii) Connect the output/s as required via a 50 Ω co-axial cable to the measuring instrument. It is recommended that, if the length of the output cable exceeds 1 metre, the line be terminated in an impedance of 50 Ω.

Both outputs are available to be used simultaneously.

(iii) Switch on the supply. The instrument neon light (SUPPLY) should illuminate.

(iv) Check that the OUTPUT VALID lamp is illuminated, if not ascertain that the input signal is as specified in chapter 1.2 and that the input and output terminations are correctly matched.

NOTE - Under certain conditions (generally with frequencies greater than 250 MHz) a correct output may be obtained without illumination of the OUTPUT VALID lamp. The TF 2422 may be used in this mode but verification of the output validity should be made.

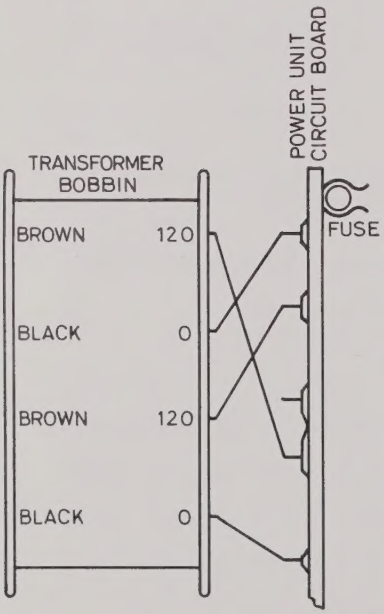


Fig 2.1 200-250 V a.c. Transformer Tapping

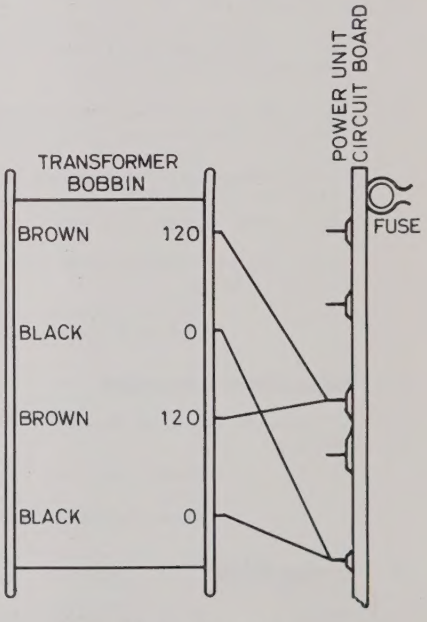


Fig 2.2 100-125 V a.c. Transformer Tapping

Note:- If the Mains voltage setting is altered ensure that the rear panel mounted mains fuse is of the correct rating; Fuse type numbers are given under maintenance.

Voltage Range	Fuse Rating	Fuse Type
200 - 250 V a.c.	250 mV)	Mag./Nickel
100 - 125 V a.c.	500 mV)	Slow-Blow

Chapter 3

Circuit description

3.1 INTRODUCTION

This section should be read in conjunction with the inter-unit wiring diagram Fig. 7.5 which shows the plug-in stages (i.e. power unit and printed boards) in block schematic form. Each block contains the title, type number and circuit diagram number of the stage.

The four stages, Power Supply Unit, 300 MHz Divider, 40 MHz Divider and the Lamp Driver are all on separate P.C.B.

3.2 POWER SUPPLY UNIT P.C.B. 55/280 (Fig 7.1)

The mains supply is fed via the three-core cable to terminal 2 (LIVE) and terminal 1 (NEUTRAL) of the power supply unit. The earth wire is taken to chassis via terminal 3.

Within the power unit the supply lines are routed to edge-connector contacts 2 (LIVE) and 1 (NEUTRAL), and returned via the double-pole 'SUPPLY ON' switch S1 to contacts 3 (LIVE) and 4 (NEUTRAL). The neon indicator lamp LP2 is powered via resistor R1 when switch S1 is closed.

From the power unit edge-connector contacts 3 and 4, the Live and Neutral lines (respectively) are applied to the split primary winding of mains transformer T1.

A mains fuse FS1 is incorporated in the Live line.

Series or parallel connection of T1 primary windings enable the instrument to be operated from a 200 - 250 V or 100 - 125 V a.c. supply. A centre-tapped secondary winding on T1 provides 9.1 V - 0 V - 9.1 V for the full-wave rectifier circuits D1/D2 and D3/D4; C1 and C4 being the respective reservoir capacitors. The positive line is connected to chassis and forms the 0 V rail (available at edge-connector contact 8). A further supply line is derived via low-pass filter C5 and R7 from the rectified output of diodes D3 and D4; this line is held at -10 V (approx. with respect to chassis) by the action of Zener diode D6.

Zener diode D5 with its load resistor R10 provides a reference potential (pre-settable by R4) for the differential amplifier containing transistors TR4 and TR3. This amplifier compares the potential of the -5.2 V line (available at edge-connector contact 7) with the preset reference potential.

The differential amplifier controls the base voltage of the driver transistor TR2 which in turn controls the series transistor TR1. Therefore any fluctuation of the -5.2 V rail is detected by the differential amplifier for TR2 and TR1 to be controlled for stabilization of the rail voltage.

3.3 300 MHz DIVIDER P.C.B. 55/180 (Fig 7.2)

Input signals are presented to socket SK1 and pass via the frequency response compensating network (R5, C8) and coupling capacitor C7 to pin 8 of integrated circuit X1. Components L1, R1 and R2 are used to provide a constant input impedance of approximately 50 Ω.

Logic elements X1 and both elements of X2 are interconnected to form a wide-band amplifier having a gain of approximately 125. To enable large variations in signal amplitude to be accommodated, feedback from transistor TR1 is applied to pin 8 of element X1 and pins 4, 5, 6 and 7 of element X2 to maintain the correct potential at pin 8 of the integrated circuit flip-flop* X3 irrespective of signal amplitude.

The feedback voltage is produced as follows:
The d.c. component present in the signal at pin 8 of element X3 is passed via low-pass filter R11, C14 and C32 to the base of TR3. The differential d.c. amplifier comprising TR1, TR2 and TR3 is used to compare the potential of the d.c. component with the reference potential, preset at R22.

From the collector of TR1 the amplified signal is then passed:

i) via low-pass filter (C20, C22 and R18) and feedback resistor R15 to pin 8 of element X1.

ii) via low-pass filter R17 and R13 to pins 4, 5, 6 and 7 of the subsequent X2 element.

The d.c. voltage level at the input of X3 is therefore determined by the setting of the reference voltage potentiometer R22. From element X2 (pin 12) an output is taken via C23 to the d.c. clamp (diode D2) which clamps the signal to a pre-determined level set by R22 (Fig. 7.4). A d.c. signal output proportional to peak-to-peak input signal amplitude is available at contact 7 (O/P3) for control of the lamp driver circuit.

From element X2 (pin 13) the amplified signal is presented to the ECL 'D' flip-flop X3** which is connected to operate as a '÷2 stage' providing Q and $\overline{Q}$ outputs.

From flip-flop X3 pin 10 an output is taken via low-pass filter C1, C2 and R3 to contact 5 (O/P1) for the lamp driver board. A second output of X3 (pin 2) is taken via a similar filter (C3, C4 and R4) to contact 6 (O/P2) for the lamp driver board. Both of these mean level d.c. outputs are available to drive the 'Valid Lamp' circuitry (Fig. 7.4).

* or bistable.

** ECL 'D' flip-flop = Emitter coupled Logic 'D' flip-flop.

With the instrument dividing correctly, the mean d.c. levels at O/P1 and O/P2 are identical. Should miscounting occur due to the applied input signal being unsuitable, a difference between the mean d.c. levels at O/P1 and O/P2 occurs.

From pin 2 of the integrated (flip-flop) circuit X3 the signal is passed to buffer stage X4 which feeds the clock pulse line of a '÷5 stage' comprising integrated circuits X5, X6 and X7. The output from this divider is applied via C25 and R29 to the base of TR4.

Transistors TR4 and TR5 form a long-tailed output amplifier which is overdriven to provide a shaped output. Transistor TR5 provides the output to socket SK2; this output consists of a rectangular wave with a mark to space ratio of approximately 2:3. From TR4 collector an output (fed via a 50 Ω strip line) is available at edge-connector contact 4 to trigger the 40 MHz divider circuit.

3.4 40 MHz DIVIDER P.C.B. 55/190 (Fig 7.3)

The 'divided down' signal at the collector of TR4 of the 300 MHz divider board, is presented to contact 3 (I/P1). This signal is applied to the base of TR1 via R2 and C1 which provide base bias and a degree of signal 'speed-up' respectively.

Transistor TR1 operates in saturated mode and acts as an interface stage (or level converter) between output levels of TR4 and TR5 (Fig. 7.2) and the TTL Logic levels of the X1 and X2 integrated circuits. The output of TR1 feeds the input of a decade frequency divider comprising, one ÷2 integrated circuit and three integrated circuits inter-connected for frequency division by 5.

From integrated circuit element X2 (pin 8) the signal is taken via R4 to the over-driven differential amplifier TR2 and TR3 whose output consists of a rectangular waveform of mark-to-space ratio 2:3 (approximately).

3.5 LAMP DRIVER P.C.B. 55/380 (Fig 7.4)

The mean d.c. levels derived from the Q and $\overline{Q}$ outputs of the 300 MHz divider board are received at contact 1 (I/P1) and contact 2 (I/P2).

The amplitude-dependent signal from the diode clamp circuit of the 300 MHz divider board is received at contact 3 (I/P3) and is applied to the base of TR5.

Provided that the instrument is operating correctly the following conditions exist:

i) The d.c. potential applied at I/P2 is identical to that at I/P1, thus both transistors of the differential amplifier (TR1 and TR2) are biased off.

The resultant 'high' potentials at the collectors of TR1 and TR2 'hold-off' transistors TR4 and TR3.

(ii) The mean d.c. input voltage proportional to signal level applied via I/P3 to the base of TR5, is sufficient to bias the transistor off.

Transistors TR3, TR4 and TR5 together with TR6 form a negative OR-gate. With transistors TR3, TR4 and TR5 cut-off, transistor TR8 in the TR7-TR8 Schmitt trigger stage is conducting. For this condition lamp driver transistors TR9 and TR10 draw current via the external 'Output Valid' lamp connected between edge connector contact 7 (of the lamp driver board) and edge connector contact 6 of the power unit (Fig. 7.1). Diode D1 is included for temperature compensation.

To minimise lamp flicker, the trigger signal for TR7 is partially integrated by capacitor C1. The lamp driver stage operates as a constant current source and thus extends the life of the 'Output Valid' lamp.

If the instrument fails to respond correctly to input signals, a resultant voltage difference occurs between I/P1 and I/P2; therefore, either TR1 or TR2 conducts and the negative OR-gate (comprising TR3, TR4, TR5 and TR6) is enabled* causing the Schmitt trigger to change state and the lamp driver stage to turn off the 'Output Valid' lamp. If the peak-to-peak value of the applied signal is too low, the base potential of TR5 is also low which thus 'enables' the negative OR-gate, resulting in the 'Output Valid' lamp off condition.

* enabled = gate biased to operable condition.

Chapter 4

Maintenance

4.1 INTRODUCTION

This section contains information for keeping the TF 2422 300 MHz Divider in good working order.

The equipment is aligned during manufacture and in general should not require re-alignment except following the replacement or repair of a component or sub-assembly. Re-alignment instructions are given in Chapter 5.

4.2 ACCESS

The interior of the instrument is readily accessible by the removal of the 'U' shape cover after releasing the 4 pozi-drive screws near the base.

CAUTION

Care must be taken when operating the instrument with the cover removed, especially in the proximity of the power supply circuit.

4.2.1 Screws

The screws used in this instrument are of the I.S.O. Metric type.

4.3 FUSE REPLACEMENT

CAUTION

Ensure that the instrument is disconnected from the mains supply before attempting to change a mains or L.T. (5.2 V line) fuse.

(a) Mains Fuse (FS1)

The mains - fuse holder is accessible on the rear panel of the instrument.

For 200-250 V a.c. operation, a slow-blow 250 mA fuse (Part No. FPP/Z50447/1) should be fitted.

For 100-125 V a.c. operation, a slow-blow 500 mV fuse (Part No. FPP/Z50447/2) should be fitted.

(b) Low Tension Fuse (FS2)

To gain access to the L.T. fuse, withdraw the four pozi-drive retaining screws and remove the cover. The fuse holder is

mounted on the component side of the power unit circuit board. Refer to Layout Diagram fig 5.1.

A 1 A fuse (Part No. FPP/Z50447/3) should be fitted.

4.4 'OUTPUT VALID' INDICATOR LAMP REPLACEMENT

Access to this indicator lamp is obtained by unscrewing the amber lens cap from the front of the instrument. When changing the lamp, care should be taken to avoid loss of the small adaptor which is contained within the indicator.

4.5 MAINS INDICATOR NEON REPLACEMENT

Should it be necessary to fit a new neon indicator first ensure that the mains supply is disconnected; then proceed as follows:

(i) Remove the instrument cover by withdrawing its four pozi-drive retaining screws.

(ii) Carefully note the position of the two neon leads then unsolder both leads from the mains switch.

(iii) Remove the neon securing-clip (at rear of front panel). Withdraw neon and fit replacement, connect and solder both leads from the new neon in the correct positions; refit instrument cover.

Chapter 5

Repair

5.1 INTRODUCTION

This chapter contains information for the location and repair of faults. Performance limits quoted are for guidance only and should not be taken as guaranteed performance specifications unless they are also quoted in the Data Summary (chapter 1.2).

See Maintenance (chapter 4) for advice on screws, access and layout.

In the case of difficulty, please write to or phone the Marconi Instruments Service Division or nearest representative, quoting the type and serial number of the instrument. If the instrument is being returned for repair please indicate clearly the nature of the fault or the work to be carried out.

5.1.1 Test Equipment Required

(a)	TF 2670	Digital Multimeter or suitable voltmeter
(b)	TF 801D/1	Signal Generator or equivalent
(c)	TF 2210	Oscilloscope or equivalent
(d)	50 Ω BNC cable and 50 Ω termination	
(e)	2414A	Counter/Timer or equivalent
(f)	BNC - N adapters	

5.2 LOW VOLTAGE SETTING

Equipment (a)

(i) Connect the positive lead of the TF 2670 to the 0 V terminal adjacent to the co-axial connector at the rear of the 55/180 P.C.B. and the negative lead to the -5.2 V terminal of the potentiometer R22.

(ii) Switch on the TF 2422 and adjust R4 on the 55/280 P.C.B. for a reading of 5.2 V ± 0.02 V.

5.3 INPUT IMPEDANCE

By adjustment of L1 in production the input impedance of the TF 2422 is set at 50 Ω ± 10%.

Special test equipment is required and if the value of L1 is changed when a repair is being made to this circuit, it is recommended that the instrument be returned to Marconi Instruments for re-alignment (see chapter 5.1)

5.4 OUTPUT WAVEFORMS

Equipment (b) (c) (d) and (e)

(i) With the TF 801D/1 Signal Generator set to 100 MHz, connect the signal to the TF 2422 input.

(ii) Connect the ÷100 output of the TF 2422 to the TF 2414A and adjust the TF801D/1 output until the counter gives the correct reading.

(iii) Disconnect the TF 2414A and connect the TF 2210 Oscilloscope to the ÷100 output via the 50 Ω co-axial cable and the 50 Ω termination.

(iv) Switch the TF 2210 timebase to 200 ns/cm range with the vertical sensitivity to 0.2 V/cm. The waveform should have a peak-to-peak voltage of equal to, or greater than 1 V.

(v) Ensure that the mark space ratio is 2:3 as illustrated below.

(vi) Set the time base to 5 ns/cm and check that the 10% to 90% rise and fall times are less than 10 µs.

(vii) With the TF 801D/1 set to 10 MHz and measuring the ÷10 output repeat (ii) to (v).

NOTE - If the waveform characteristics are not as stated in (iv) to (vi) the components should be checked for correct function and value.

5.5 INPUT SENSITIVITY

Equipment (b) (d) (e) and (f)

(i) Connect the TF 801D/1 set to 300 MHz/100 mV to the TF2422 input via the 50 Ω co-axial cable.

(ii) Connect the ÷100 output of the TF 2422 via a 50 Ω co-axial cable terminated in 50 Ω to the TF 2414A input.

(iii) The counter should indicate the correct frequency. If not set R22 on the 55/180 P.C.B. fully clockwise and then rotate anti-clockwise until a correct stable reading is obtained.

(iv) Reduce the generator output until the counter begins to mis-count. Rotate R22 (55/180) anti-clockwise until a correct stable reading is obtained.

(v) Repeat (iv) until optimum sensitivity is reached. Note the generator amplitude which just gives correct division. This will be referred to as Vmin.

(vi) Set the generator amplitude to 1.25 x Vmin. Rotate R22 (55/180) clockwise, until the counter gives a correct stable reading.

(vii) Reduce the generator amplitude below Vmin and then slowly increase amplitude until the counter shows a correct stable reading. The amplitude of the generator output should be between 1.25 x Vmin and 1.30 x Vmin and be less than 25 mV.

(viii) Increase the generator amplitude to 3 V and check for correct division.

(ix) If incorrect results are obtained from (viii) repeat (vii) rotating R22 anti-clockwise through the point of optimum sensitivity to achieve similar results as in (vii) so that the requirements of (viii) are also met.

(x) Reduce the generator frequency to 12 MHz, set amplitude to 3 V and check for correct division.

(xi) If incorrect results are obtained from (x) repeat (vii) and (viii) at 300 MHz until the requirements of (x) at 12 MHz are also met.

5.6 PACKAGING FOR RESHIPMENT

In the event of the equipment being returned for servicing it should be packed in the original shipping carton and packing material. If this is not available wrap the instrument in heavy paper or plastic and place in a rigid outer box of wood, fibreboard or very strong corrugated cardboard. Use ample soft packing to prevent movement. Provide additional support for projecting parts to relieve these of unnecessary shock. Close the carton securely and seal with durable tape. Mark the shipping container FRAGILE to ensure careful handling.

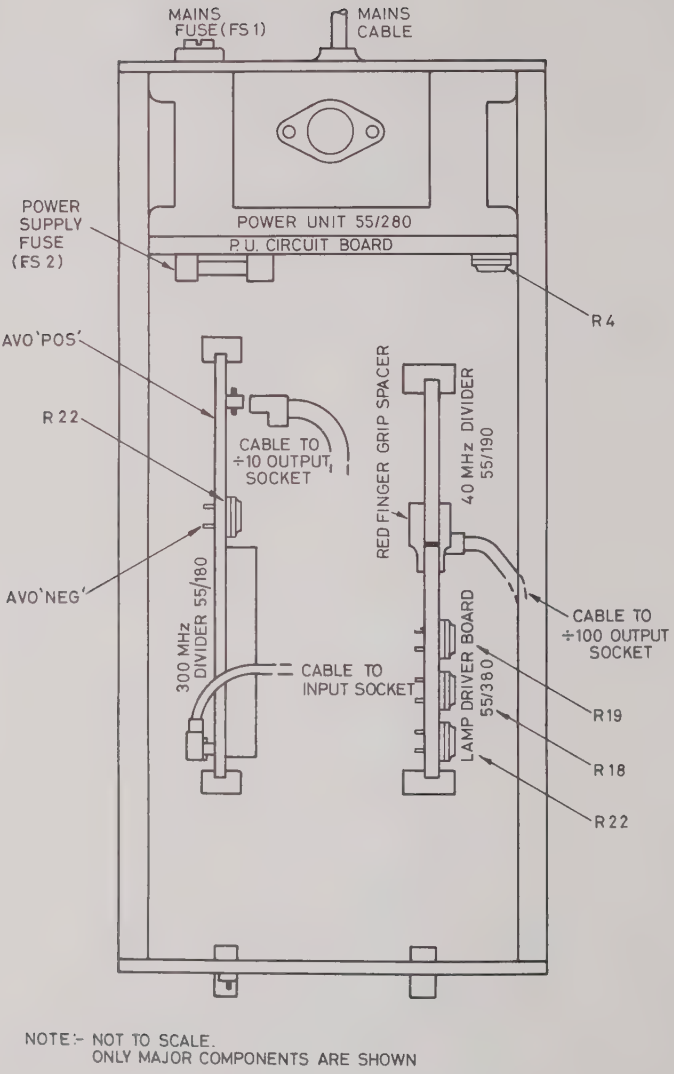


Fig 5.1 P.C.B. and Preset Control Location

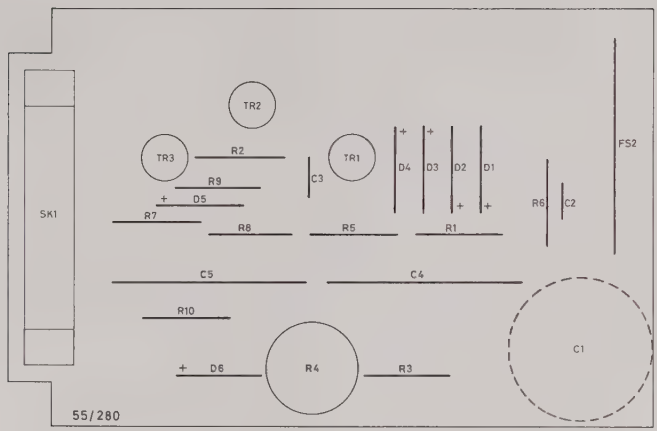


Fig 5.2 Power Supply Unit P.C.B. 55/280
Component Location

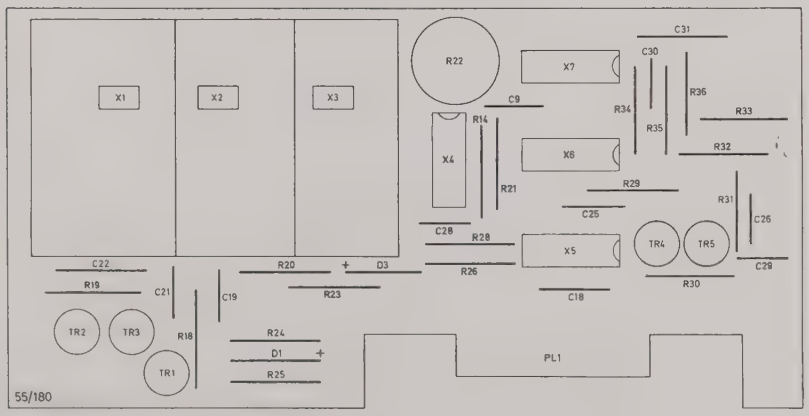


Fig 5.3 300 MHz Divider P.C.B. 55/180
Component Location

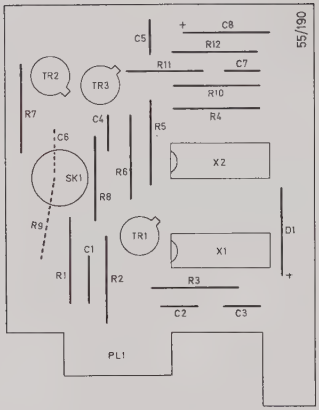


Fig 5.4 40 MHz Divider P.C.B. 55/190
Component Location

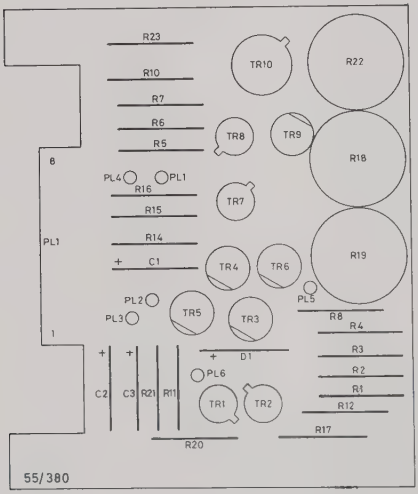


Fig 5.5 Lamp Driver P.C.B. 55/380
Component Location

Chapter 6

Replaceable parts

6.1 INTRODUCTION

This chapter lists the replaceable parts in alpha-numerical order of circuit references, sub-divided into five sections in the order shown below. The associated circuit diagrams are also indicated.

Power Supply Unit	X0 - Fig. 7.1
300 MHz Divider Board	X1 - Fig. 7.2
40 MHz Divider Board	X2 - Fig. 7.3
Lamp Driver Board	X3 - Fig. 7.4
Chassis Assembly	X4 - Fig. 7.5

The following abbreviations are used in the parts list,

C	capacitor	PL	plug
D	diode	R	resistor
FS	fuse	S	switch
IC	integrated circuit	SK	socket
Lin	linear	T	transformer
LP	lamp	TR	transistor

6.2 ORDERING

When ordering replacement or spare parts, address the order to our Service Division (for address see rear cover) or nearest representative. Please specify the following information for each part required:-

(i) Type and serial number of instrument
(ii) Circuit reference number
(iii) Description
(iv) M.I. Part number (preceded by FPP)

If a part is not listed, state its function, location and description when ordering.

Spares supplied against M.I. part numbers are electronically interchangeable with those originally fitted, but may not always be identical.

6.3 PARTS LIST

Circuit Reference	Description	M.I. Code No. FPP/
POWER SUPPLY UNIT (Circuit Diagram Fig. 7.1) (When ordering, prefix circuit reference XO)		
Capacitors -		
C1	2000 uF 16 V	X20643/68
C2/3	0.047 pF +50% -25%	X20641/55
C4/5	100 uF 25 V	X20643/15
Diodes -		
D1 - 4	1N4001	X20639/45
D5/6	BZY88/C5V6	X20639/30
Fuses -		
FS1	For 200-250 V a.c. operation: 250 mA Slow Blow	Z50447/1
	For 100-125 V a.c. operation: 500 mA Slow Blow	Z50447/2
FS2	1 A	Z50447/3
Resistors -		
R1	1 kΩ ±5% ¼ W	X50500/49
R2	2.2 kΩ ±5% ¼ W	X50500/57
R3	6.8 kΩ ±5% ¼ W	X50500/69
R4 (Variable)	1 kΩ ±20% ¼ W (LIN)	X20999/58
R5	22 kΩ ±5% ¼ W	X50500/81
R6	180 Ω ±5% ¼ W	X50500/31
R7/8	270 Ω +5% ¼ W	X50500/35
R9	3.3 kΩ ±5% ¼ W	X50500/61
R10	1 kΩ ±5% ¼ W	X50500/49
Transformer -		
T1	Albion OZ293	Y51786
Transistors -		
TR1	40250	X20638/60
TR2 - 4	V435	X20638/72

Circuit Reference	Description	M.I. Code No. FPP/

300 MHz DIVIDER BOARD (Circuit Diagram Fig. 7.2)
(When ordering, prefix circuit reference X1)

Capacitors -

C1	0.047 µF +50% -25%	X20641/55
C2/3	1000 pF +80% -20%(Feed Through)	Y50525/2
C4	0.047 µF +50% -25%	X20641/55
C5	10 pF $\pm\frac{1}{2}$ pF	Y20644/14
C6	5 pF ±1 pF	Y20644/3
C7	0.001 µF ±10%	Y20641/56
C8	33 pF ±2%	Y20644/12
C9	4.7 pF ±20%	Y50509/22
C10/11	0.047 µF +50% -25%	X20641/55
C12	47 µF 6 V	Y22776/14
C13/14	1000 pF +80% -20%(Feed Through)	Y50525/2
C15	0.047 µF +50% -25%	X20641/55
C16	47 µF 6 V	Y22776/14
C17-19	0.047 µF +50% -25%	X20641/65
C20	1000 pF +80% -20%(Feed Through)	Y50525/2
C21	0.047 µF +50% -25%	X20641/55
C22	47 µF 6 V	Y22776/14
C23	0.047 µF +50% -25%	X20641/55
C24	1000 pF +80% -20%(Feed Through)	Y50525/2
C25	0.047 µF +50% -20%	X20641/31
C26	0.047 µF +50% -25%	X20641/55
C27	1000 pF +80% -20%(Feed Through)	Y50525/2
C28-30	0.047 µF +50% -25%	X20641/55
C31	47 µF 6 V	Y22776/14
C32	0.047 µF +50% -25%	X20641/55

Diodes -

D1	1N4009	X20639/41
D2	CAY11	X20639/44
D3	1N4009	X20639/41

Integrated Circuits -

IC1/2	MC1660S	X50520/14
IC3	MC1670S	X50520/15
IC4	MC1023P	X50520/16
IC5-7	MC1034P	X50520/17

Circuit Reference	Description	M.I. Code No. FPP/
300 MHz DIVIDER BOARD (continued)		
Resistors -		
R1	100 Ω ±5% ¼ W	X50500/25
R2	120 Ω ±5% ¼ W	X50500/27
R3/4	1.5 kΩ ±10% 0.2 W	X50514/27
R5/6	470 Ω ±10% 0.2 W	X50514/21
R7	270 Ω ±10% 0.2 W	X50514/18
R8	47 Ω ±10% 0.2 W	X50514/9
R9/10	270 Ω ±10% 0.2 W	X50514/18
R11	1.5 kΩ ±10% 0.2 W	X50514/27
R12/13	470 Ω ±10% 0.2 W	X50514/21
R14	270 Ω ±5% ¼ W	X50500/35
R15	470 Ω ±10% 0.2 W	X50514/21
R16	270 Ω ±10% 0.2W	X50514/18
R17	470 Ω ±10% 0.2 W	X50514/21
R18	1.2 kΩ ±5% ¼ W	X50500/51
R19	150 Ω ±5% ¼ W	X50500/29
R20	1.5 kΩ ±5% ¼ W	X50500/53
R21	10 kΩ ±5% ¼ W	X50500/73
R22 (Variable)	2.2 kΩ 1 W (Lin)	X20999/49
R23	5.6 kΩ ±5% ¼ W	X50500/67
R24	680 Ω ±5% ¼ W	X50500/45
R25	1 kΩ ±5% ¼ W	X50500/49
R26	330 Ω ±5% ¼ W	X50500/37
R27	27 kΩ ±10% 0.2 W	X50514/42
R28	680 Ω ±5% ¼ W	X50500/45
R29	470 Ω ±5% ¼ W	X50500/41
R30	68 Ω ±5% ¼ W	X50500/21
R31	47 Ω ±5% ¼ W	X50500/17
R32	390 Ω ±5% ¼ W	X50500/39
R33	2.2 kΩ ±5% ¼ W	X50500/57
R34	1 kΩ ±5% ¼ W	X50500/49
R35	39 Ω ±5% ¼ W	X50500/15
R36	390Ω ±5% ¼W	X50500/39
Sockets -		
SK1/2	B.N.C. Miniature	X50508/12
Transistors -		
TR1	U15718/1	X20638/55
TR2/3	V435	X20638/72
TR4/5	U15718/1	X20638/55

Circuit Reference	Description	M.I. Code No. FPP/
40MHz DIVIDER BOARD (Circuit Diagram Fig. 7.3) (When ordering, prefix circuit reference X2)		
Capacitors -		
C1	100 pF ±10%	Y50505/7
C2/3	0.047 µF +50% -25%	X20641/55
C4	0.001 µF ±10%	X20641/56
C5-7	0.047 µF +50% -25%	X20641/55
C8	47 µF 6 V	Y22776/14
Diodes -		
D1	1N4001	X20639/45
Integrated Circuits -		
IC1/2	MC3062P	X50520/11
Resistors -		
R1	68 Ω ±5% ¼ W	X50500/21
R2	820 Ω ±5% ¼ W	X50500/47
R3	220 Ω ±5% ¼ W	X50500/33
R4	470 Ω ±5% ¼ W	X50500/41
R5	820 Ω ±5% ¼ W	X50500/47
R6	33 Ω ±5% ¼ W	X50500/13
R7	47 Ω ±5% ¼ W	X50500/17
R8	390 Ω ±5% ¼ W	X50500/39
R9	2.2 kΩ ±5% ¼ W	X50500/57
R10	1 kΩ ±5% ¼ W	X50500/49
R11	39 Ω ±5% ¼ W	X50500/15
R12	390 Ω ±5% ¼ W	X50500/39
Sockets -		
SK1	B.N.C. Miniature	X50508/12
Transistors -		
TR1	V405A	X20638/65
TR2/3	U15718/1	X20638/55

Circuit Reference	Description	M.I. Code No. FPP/
LAMP DRIVER BOARD (Circuit Diagram Fig. 7.4) (When ordering, prefix circuit reference X3)		
Capacitors -		
C1	10 µF 20 V	Y22776/17
C2/3	47 µF 6 V	Y22776/14
Diodes -		
D1	1N4001	X20639/45
Resistors -		
R1/2	2.2 kΩ ±5% ¼ W	X50500/57
R3	100 Ω ±5% ¼ W	X50500/25
R4	1.2 kΩ ±5% ¼ W	X50500/51
R5	1.5 kΩ ±5% ¼ W	X50500/53
R6	2.2 kΩ ±5% ¼ W	X50500/57
R7	10 Ω ±5% ¼ W	X50500/1
R8	3.3 kΩ ±5% ¼ W	X50500/61
R9	10 kΩ ±5% ¼ W	X50500/73
R10	120 Ω ±5% ¼ W	X50500/27
R11/12	2.2 kΩ ±5% ¼ W	X50500/57
R13	Not used	
R14	4.7 kΩ ±5% ¼ W	X50500/65
R15	2.2 kΩ ±5% ¼ W	X50500/57
R16	15 kΩ ±5% ¼ W	X50500/77
R17	1 kΩ ±5% ¼ W	X50500/49
R18 (Variable)	1 kΩ 1 W (Lin)	X20999/58
R19 (Variable)	220 Ω 1 W (Lin)	X20999/82
R20	1 kΩ ±5% ¼ W	X50500/49
R21	2.2 kΩ ±5% ¼ W	X50500/57
R22 (Variable)	1 kΩ 1 W (Lin)	X20999/58
R23	680 Ω ±5% ¼ W	X50500/45
Transistors -		
TR(1&2)*	U15718/1	X20638/55
TR3-6	V435	X20638/72
TR7/8	U15718/1	X20638/55
TR9	V435	X20638/72
TR10	2N3053	X20638/66

*Matched Pair.

Circuit Reference	Description	M.I. Code No. FPP/
CHASSIS ASSEMBLY (Circuit Diagram Fig. 7.5) (When ordering, prefix circuit reference X4)		
Indicator Lamps -		
LP1	6.5V 1W LES	Z22357
LP2	Neon Lamp	Z51400
Plugs -		
PL1-3	B.N.C. Miniature (Right Angle Connector)	X50508/11
Resistors -		
R1	270 kΩ ±5% ¼ W	X50501/11
Switches -		
S1	Mains Switch (2 pole toggle)	Z51777
Sockets -		
SK1-3	B.N.C.	X50508/23

Chapter 7

Circuit diagrams

CIRCUIT NOTES

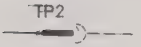
1. Component Values

Resistors	No suffix	=	ohms
	k	=	kilohms
	M	=	megohms
Capacitors	No suffix	=	microfarads
	p	=	picofarads

2. Voltages are d.c. and relative to chassis earth unless otherwise indicated.

3. Symbols

terminal post designated number 12

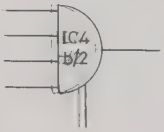


Test Point number 2

4. Integrated Circuits

In the following circuit diagrams, for reasons of clarity multi-function Integrated Circuits may be shown separated both functionally and symbolically. In such cases the circuit reference number will be suffixed by an alpha numerical designation.

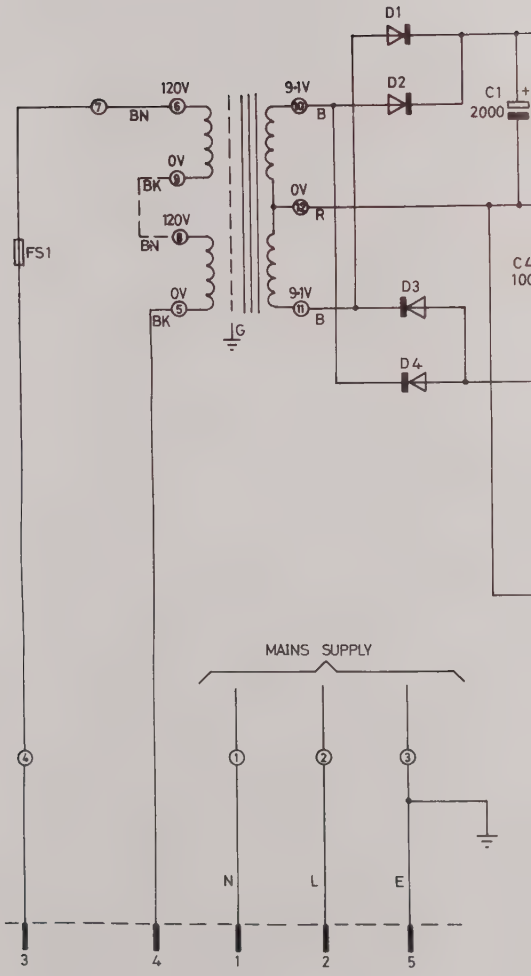
e.g.



This would mean the 'b' part of a 2 function Integrated Circuit (IC4)

5. Circuit Diagrams

Fig. 7.1	Power Supply Unit	(E68/64)
7.2	300MHz Divider	(E68/65)
7.3	410MHz Divider	(E68/62)
7.4	Lamp Driver	(E68/63)
7.5	Inter Unit Wiring	(E68/66)


D1
D2
C1
2000
120V
BN
0V
BK
120V
BN
0V
BK
FS1
9-1V
B
0V
R
9-1V
B
D3
D4
G
MAINS SUPPLY
N
L
E
3
4
1
2
5

TF 2422

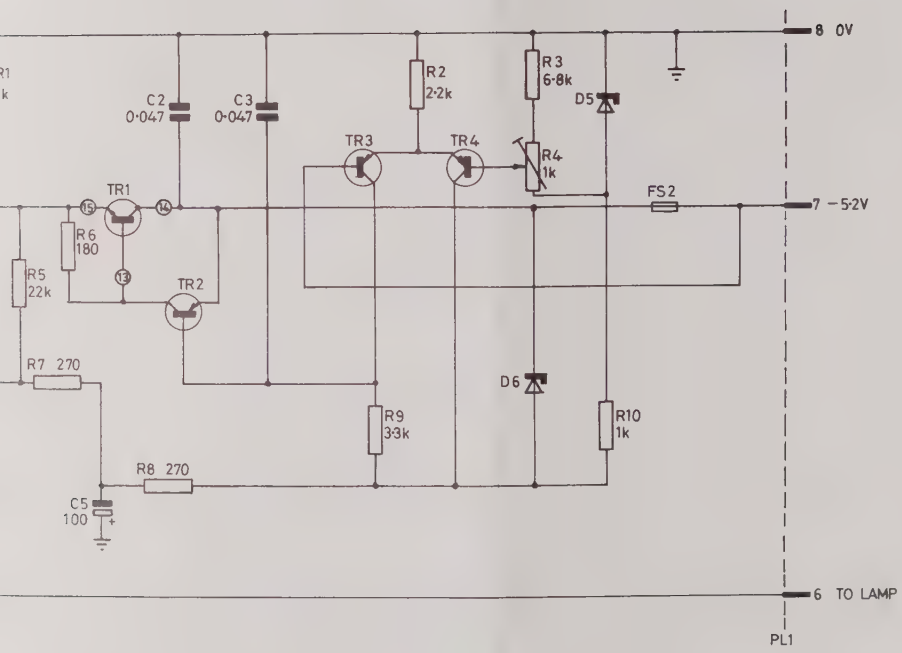
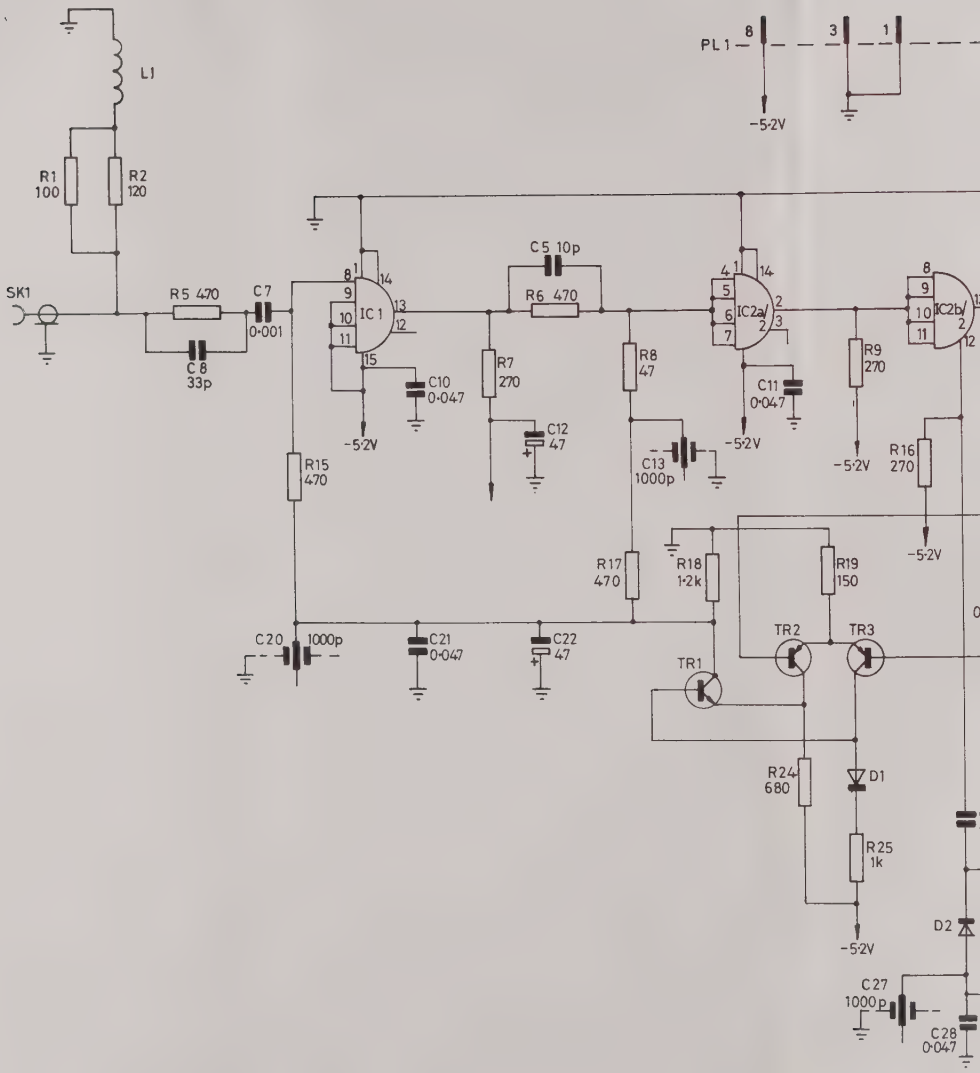


Fig 7.1 Power Supply Unit P.C.B. 55/280 Circuit Diagram (E68/64)


L1
R1 100
R2 120
SK1
R5 470
C7 0·001
C8 33p
IC1
C5 10p
R6 470
R7 270
C10 0·047
C12 47
R15 470
C20 1000p
C21 0·047
C22 47
IC2a
IC2b
R8 47
C11 0·047
C13 1000p
R9 270
R16 270
R17 470
R18 1·2k
R19 150
TR1
TR2
TR3
R24 680
D1
R25 1k
D2
C27 1000p
C28 0·047
PL1
-5·2V

TF 2422

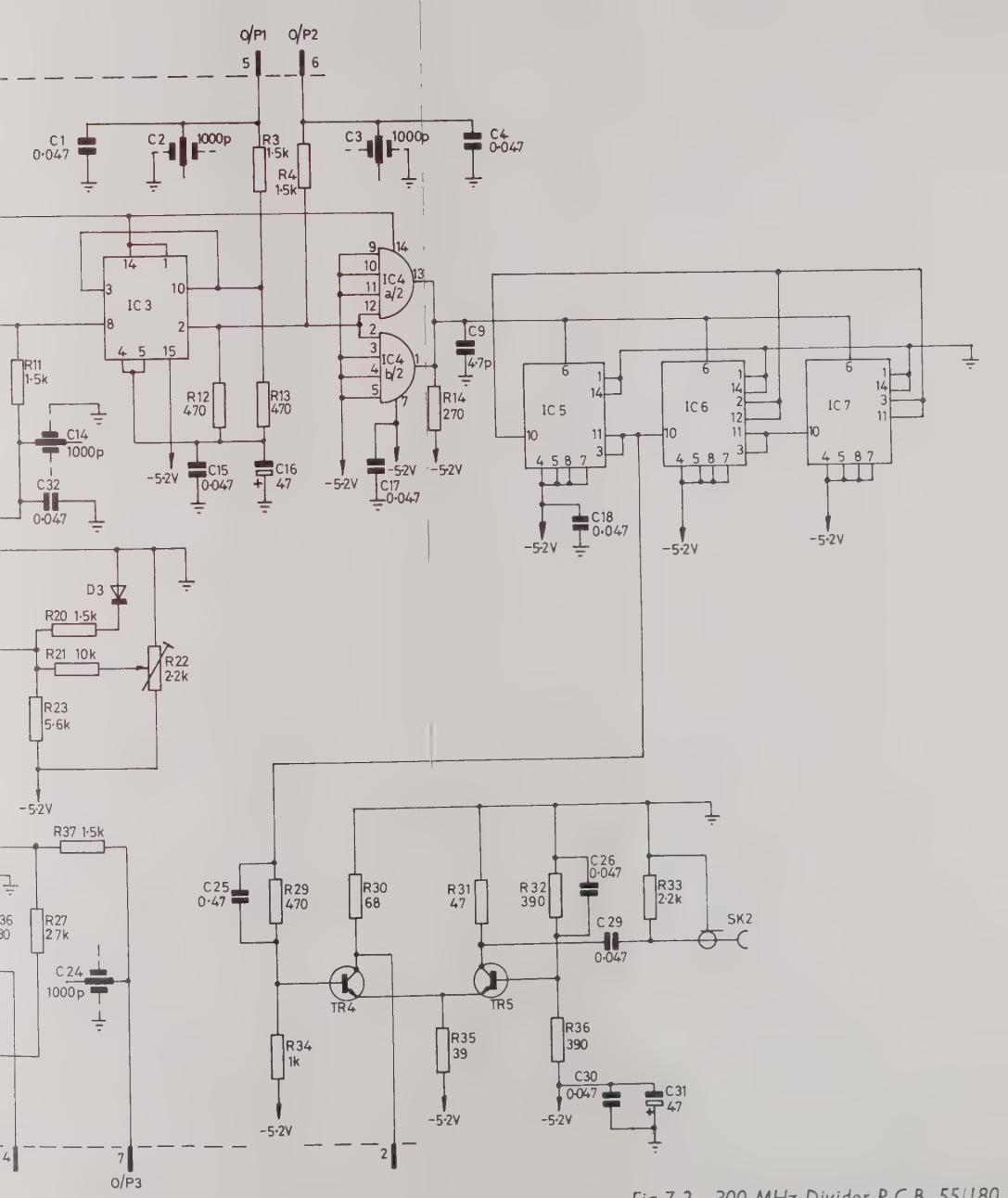
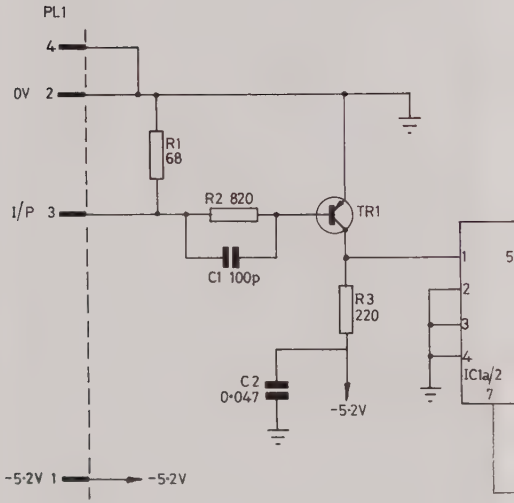


Fig 7.2 300 MHz Divider P.C.B. 55/180 Circuit Diagram (E68/65)


PL1
4
0V 2
R1
68
I/P 3
R2 820
TR1
C1 100p
R3
220
C2
0·047
-5·2V
-5·2V 1
-5·2V
1
2
3
4
IC1a/2
7

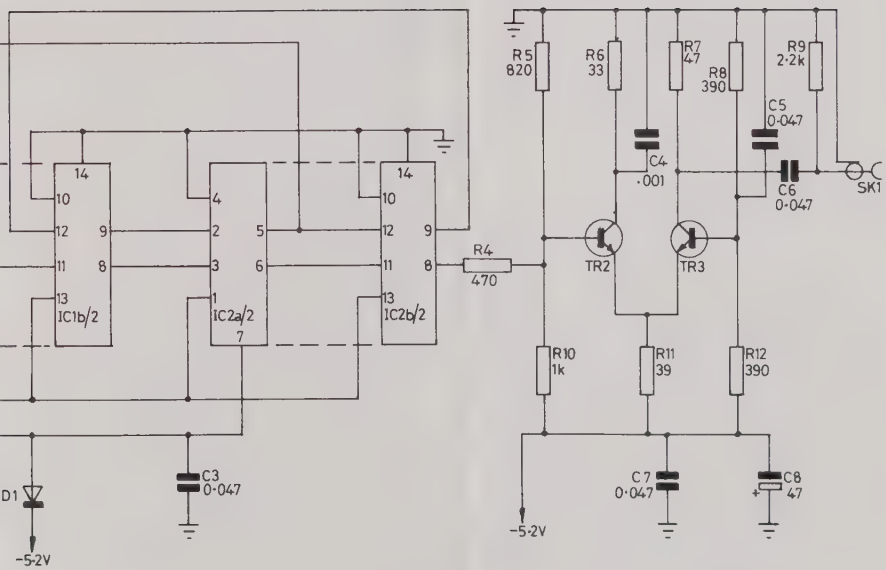
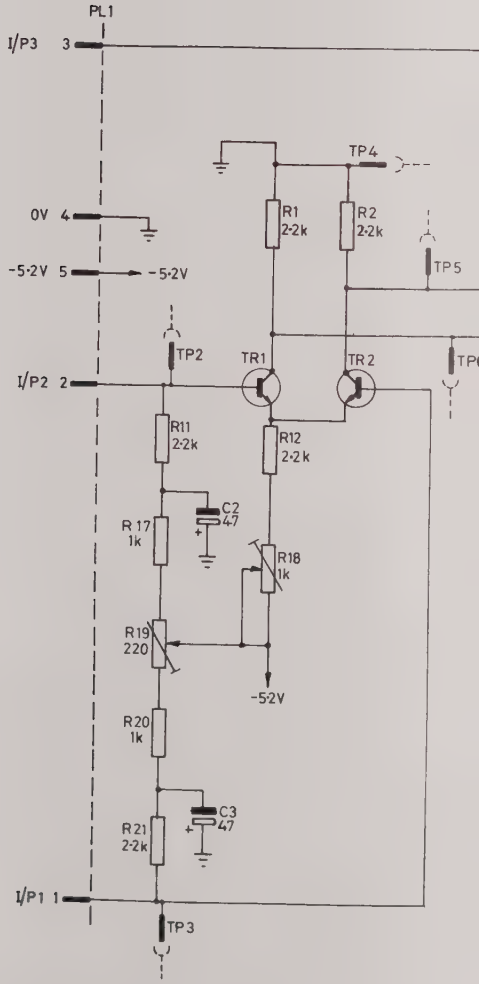


Fig 7.3 40 MHz Divider P.C.B. 55/190 Circuit Diagram (E68/62)


PL1
I/P3 3
0V 4
-5·2V 5
-5·2V
I/P2 2
I/P1 1
TP2
TP3
TP4
TP5
TR1
TR2
R1
2·2k
R2
2·2k
R11
2·2k
R12
2·2k
R17
1k
C2
47
R18
1k
R19
220
-5·2V
R20
1k
R21
2·2k
C3
47

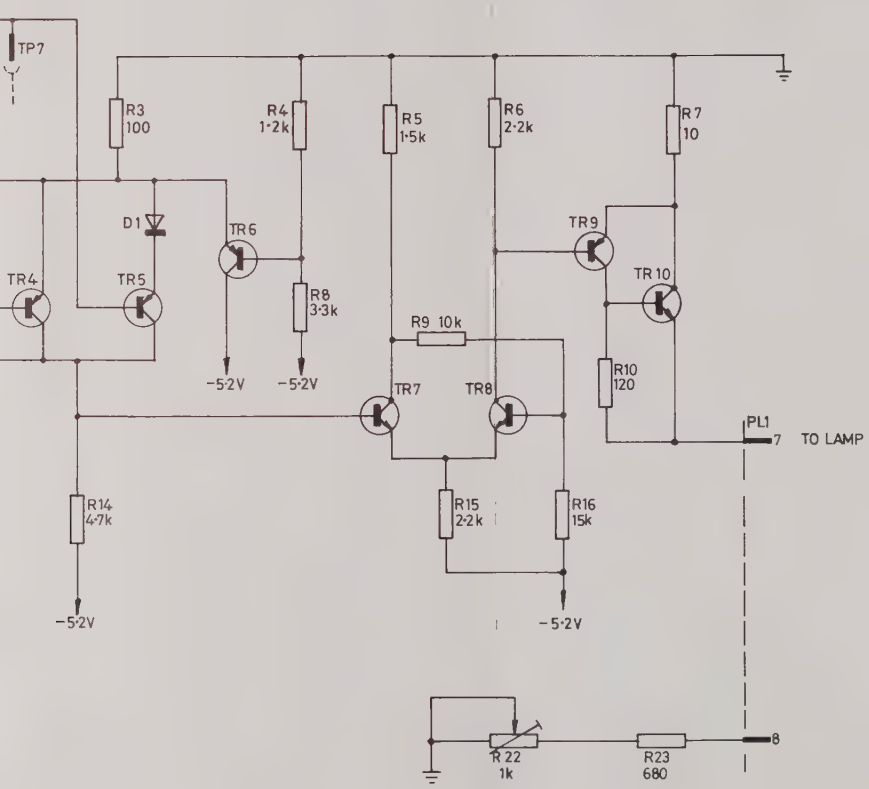
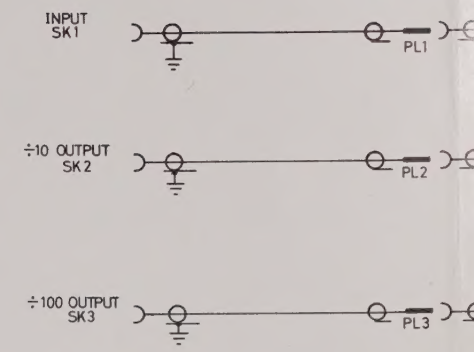
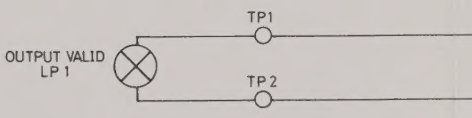
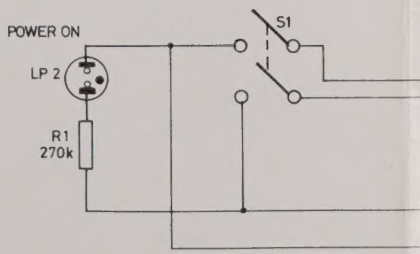


Fig 7.4 Lamp Driver P.C.B. 55/380 Circuit Diagram (E68/63)


INPUT
SK1
PL1
÷10 OUTPUT
SK2
PL2
÷100 OUTPUT
SK3
PL3


TP1
OUTPUT VALID
LP 1
TP 2


POWER ON
S1
LP 2
R1
270k

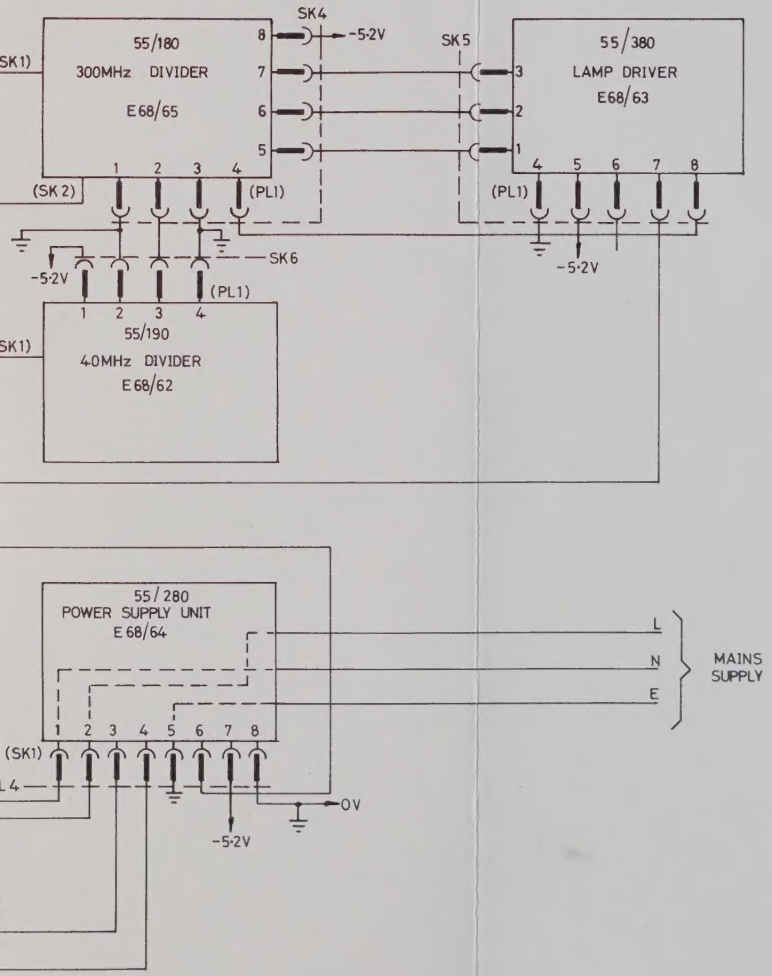


Fig 7.5 Chassis, Inter Unit Wiring Circuit Diagram (E68/66)

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